

conduction type and being connected to the input/output terminal. A second diffusion layer of the second conduction type is held at a predetermined potential. A third diffusion layer of the second conduction type is fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer. The first diffusion layer is circularly enclosed with the second and third diffusion layers.

II. THE PRIOR ART REJECTION

The Examiner asserts that the Applicant's Admitted Prior Art shown in Figures 5A and 5B discloses the invention as claimed except for "a third diffusion layer of the second conductivity type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer, the first diffusion layer being circularly enclosed with the second and third diffusion layers".

To overcome this deficiency, the Examiner relies on US Patent 5,945,713 to Voldman and is understood as asserting that one having ordinary skill in the art would be motivated to incorporate a guard ring structure "to prevent current flow to the n-channel MOSFET driver circuit, as shown by Voldman". Voldman teaches an on-chip ESD protection for semiconductor chips with mixed-voltage interface (MVI) applications and internal multiple power bus architecture (see abstract) such as a 3.3/5.0 MVI (column 2 at line 6).

Applicant respectfully submits that the rejection of record fails to meet the burden of a *prima facie* rejection under 35 USC §103(a) for at least the following reasons.

First, a proper evaluation under 35 USC §103(a) requires that the Examiner identify the difference(s) between the prior art and the present invention as claimed. For the rejection on record, since the asserted prior art is Figures 5A and 5B of the present Application, the

Examiner has the burden of first modifying that prior art to encircle n-well 104 by n-well 105 and then provide a second modification of providing a new n-well underneath n-well 105.

As best understood, the Examiner relies on n-well 12 of Voldman Figure 8 as demonstrating a guard ring of the prior art that would teach both modifications identified above. Applicant respectfully submits that Voldman n-well 12 teaches neither modification, let alone both of them.

Specifically, the n-well guard ring 12 of Voldman is described in that reference (lines 31-35 of column 7) as "placed entirely around the self-bias n-well tub and n-well diode to form a lateral well-to-well bipolar npn transistor". In contrast, the prior art shown in Figures 5A and 5B of the present Application does not have either a self-bias n-well tub or the n-well diode shown in Voldman. If an n-well corresponding to the structure shown in Voldman were somehow added to Figures 5A/5B, the transistor action described in lines 11-22 of page 2 of the specification would no longer occur, thereby defeating the purpose of the circuit.

Additionally, the action of the structure shown in Figures 5A and 5B already forms a lateral npn transistor (see page 2 at lines 16-19).

Therefore, there is no reason to modify prior art shown in Figure 5A/5B to add a guard ring to form a lateral npn transistor, since such npn lateral transistor already exists without adding the guard ring. Indeed, the reason for the encircling underlying n-well 7 of the present invention is not the formation of an npn transistor, but rather the intentional delay in charge movement so that the transistor action described for the prior art transistor occurs faster.

Second, for a motivation to combine Voldman with the Applicant's Admitted Prior Art, the Examiner relies on the phrase "n-channel MOSFET driver circuit" from lines 37-39 of

column 8 of Voldman. The complete sentence at this location actually says: "[t]he n-well ring 12 acts as a guard ring for the n-well diode to prevent to prevent current flow to the n-channel MOSFET driver circuit". It is uncertain whether this statement refers to the diode inside the n-well (labeled "NW") in Figure 8 in which is shown the diode, resistor, and PNP transistor symbols or if this phrase refers to "n-well diode" (see line 30 of column 7 of Voldman), shown unlabeled in Figure 8 but labeled in Figure 4 as "D5".

However, it does not matter which of these diode structures in Voldman is being referenced, since the prior art shown in Figures 5A and 5B of the present Application contains neither of these two diode structures. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been motivated to modify the Applicant's Admitted Prior Art in Figures 5A/5B in any way, as based on the phraseology relied upon by the Examiner, and that the rejection on record fails to provide a motivation to combine Voldman with the prior art of Figures 5A/5B.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of " ... a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the layer having a second conduction type opposite the first conduction type and being connected to the input/output terminal; a second diffusion layer of the second conduction type being held at a predetermined potential; and a third diffusion layer of the second conduction type fabricated at a bottom of the second diffusion layer, the third diffusion layer being connected to the second diffusion layer, the first diffusion layer being circularly enclosed with the second and third diffusion layers," as required by claim 1.

For this reason stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with the Voltman reference, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

The Examiner objects to the word "monotonously" in claim 3 and considers that the correct word should be "monotonically". Applicant respectfully traverses this objection. According to the definitions on the attached page 1245 of Webster's New Universal Unabridged Dictionary, 1996, the word "monotonously" has one definition meaning a "uniformity". This claim word "monotonously" is used in the specification at line 13 on page 9 and reasonably attempts to characterize the shape of the impurity concentration curve shown in Figure 2.

It is also true, as pointed out by the Examiner and as demonstrated in the definition shown on the attached page 1245 of Webster's Dictionary, that "monotonic" has a specific mathematical definition implying either an increasing or decreasing. However, Applicant's representative is also aware that a more precise mathematical definition of "monotonic" also conveys the concept that the decrease/increase proceeds in only one direction. That is, once a curve begins to increase, it is not allowed to decrease although it is allowed to be level out. Therefore, if used as claim language, the term "monotonically decreasing" might be construed, in a technically mathematical description, as inconsistent with the curve shown in Figure 2 in which the increase is shown in the left part of the curve before the curve begins to decrease.

Moreover, Applicant prefers to maintain consistency between the claim language and the terminology used in the specification.

In view of the above discussion, Applicant requests that the Examiner reconsider and

withdraw the objection to the language of claim 3.

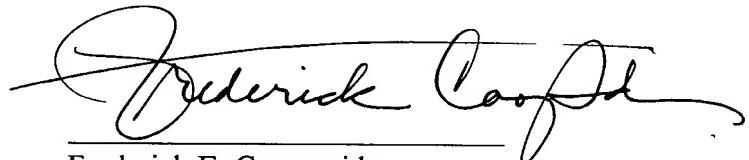
In view of the foregoing, Applicant submits that claims 1-27, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 10/4/02



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